Implementing Yasuyuki's FPHX silicon tracker in simulations with ladders

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August 18, 2015

Changes to the thickness budget

Yasuyuki proposes to change from the SVX4 chip to the FPHX chip for reading out the silicon strip tracking layers. Since the FPHX chip requires much less cooling, the material budget can be reduced.

Yasuyuki's proposed thickness budget after switching the chips:

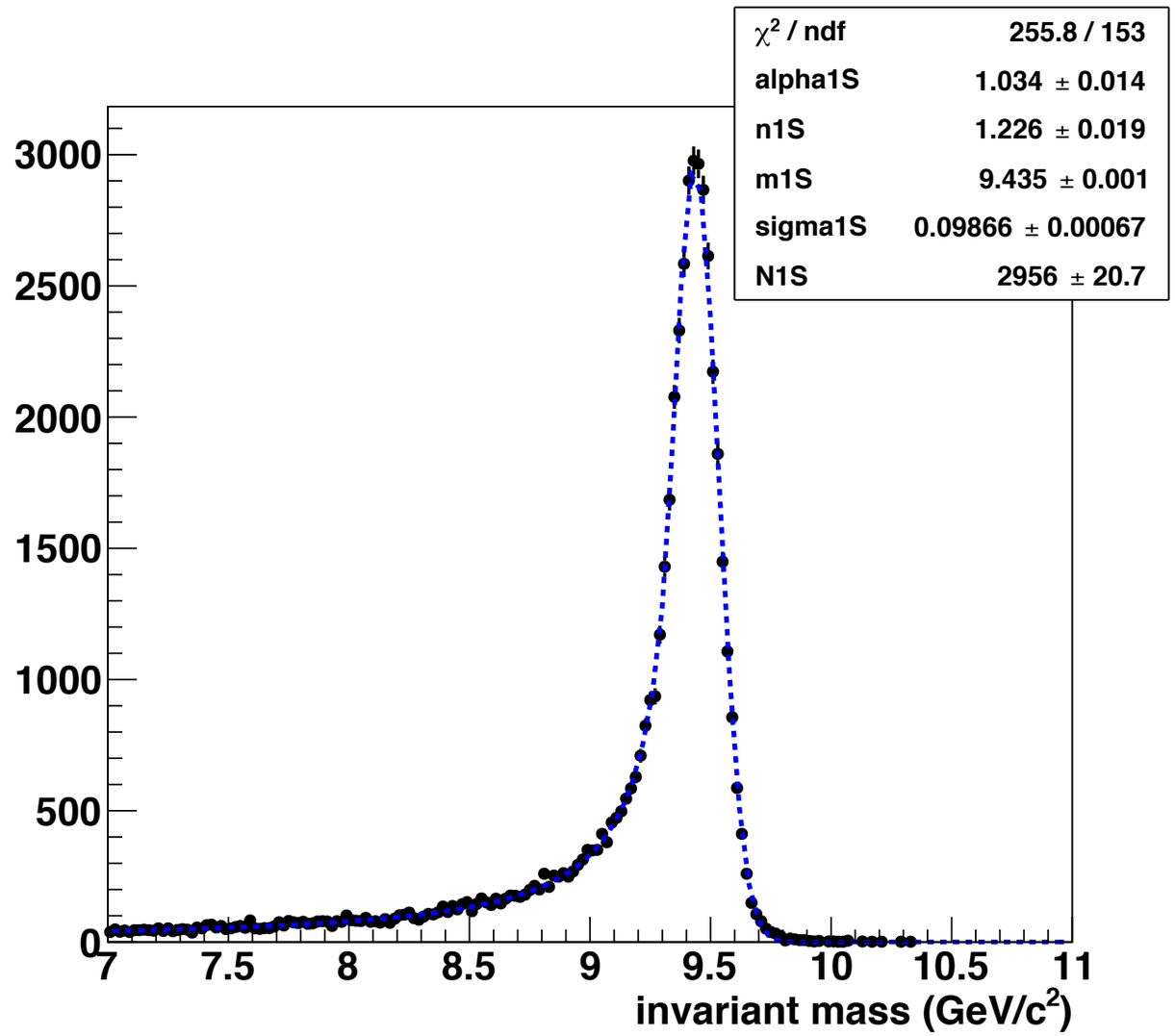
Layer	Radius	X0	
P0	2.5cm	1.3%	
P1	5.0cm	1.3%	
S0	8.0cm	2% radiation length	(For double layer S0a+S0b)
S1	32 cm	1.2%	(For double layer S1a+S1b)
S2	56 cm	1%	

I have made some estimates of the mass resolution, using this thickness budget, to try to see what the layer radii should be to achieve the needed 100 MeV Upsilon mass resolution.

Results with the cylinder cell model (64 cm outer radius)

Layer	Radius (cm)	cell size (cm x cm)	X0 (%)
P0	2.7	0.005 x 0.0425	1.3
P1	4.6	0.005 x 0.0425	1.3
S0a	7.5	0.0058 x 9.6	1.0
S0b	8.5	0.0058 x 9.6	1.0
S1a	35.0	0.0058 x 9.6	0.6
S1b	37.0	0.0058 x 9.6	0.6
S2	64.0	0.0060 x 9.6	1.0

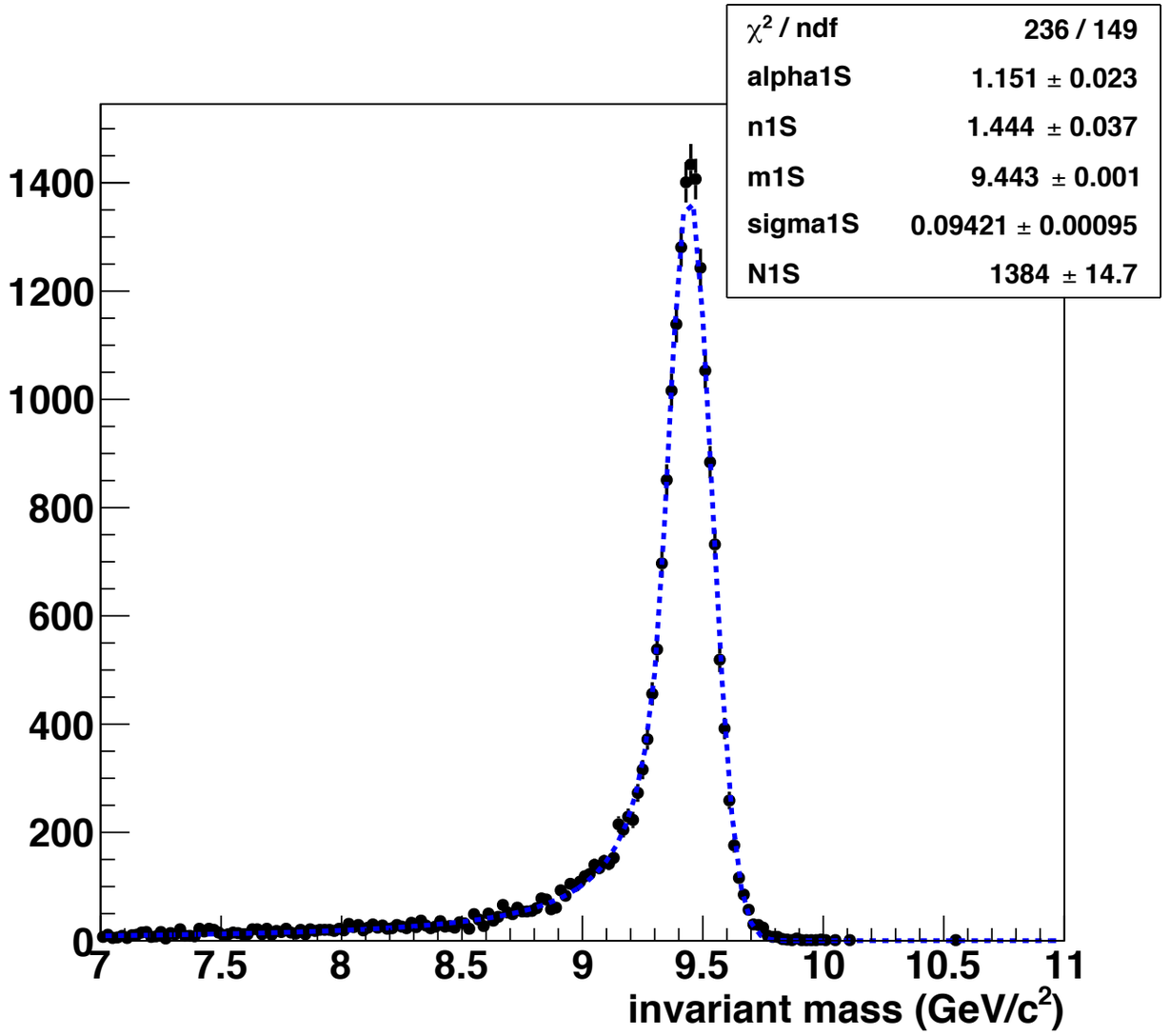
mass resolution 98.7 MeV +/- 0.7 MeV



ITS inner pixels instead of PHENIX pixels

Layer	Radius (cm)	cell size (cm x cm)	X0 (%)
P0	2.3	0.002 x 0.002	0.6
P1	3.2	0.002 x 0.002	0.6
P3	3.9	0.002 x 0.002	0.6
S0a	7.5	0.0058 x 9.6	1.0
S0b	8.5	0.0058 x 9.6	1.0
S1a	35.0	0.0058 x 9.6	0.6
S1b	37.0	0.0058 x 9.6	0.6
S2	64.0	0.0060 x 9.6	1.0

mass resolution 94.2 +/- 0.9 MeV



Creating a ladder model

The silicon tracker ladder model is created in:

coresoftware/simulation/g4simulation/g4detector/PHG4SiliconTrackerDetector

The model was made to describe the revised MIE configuration, using the SVX4 chip.

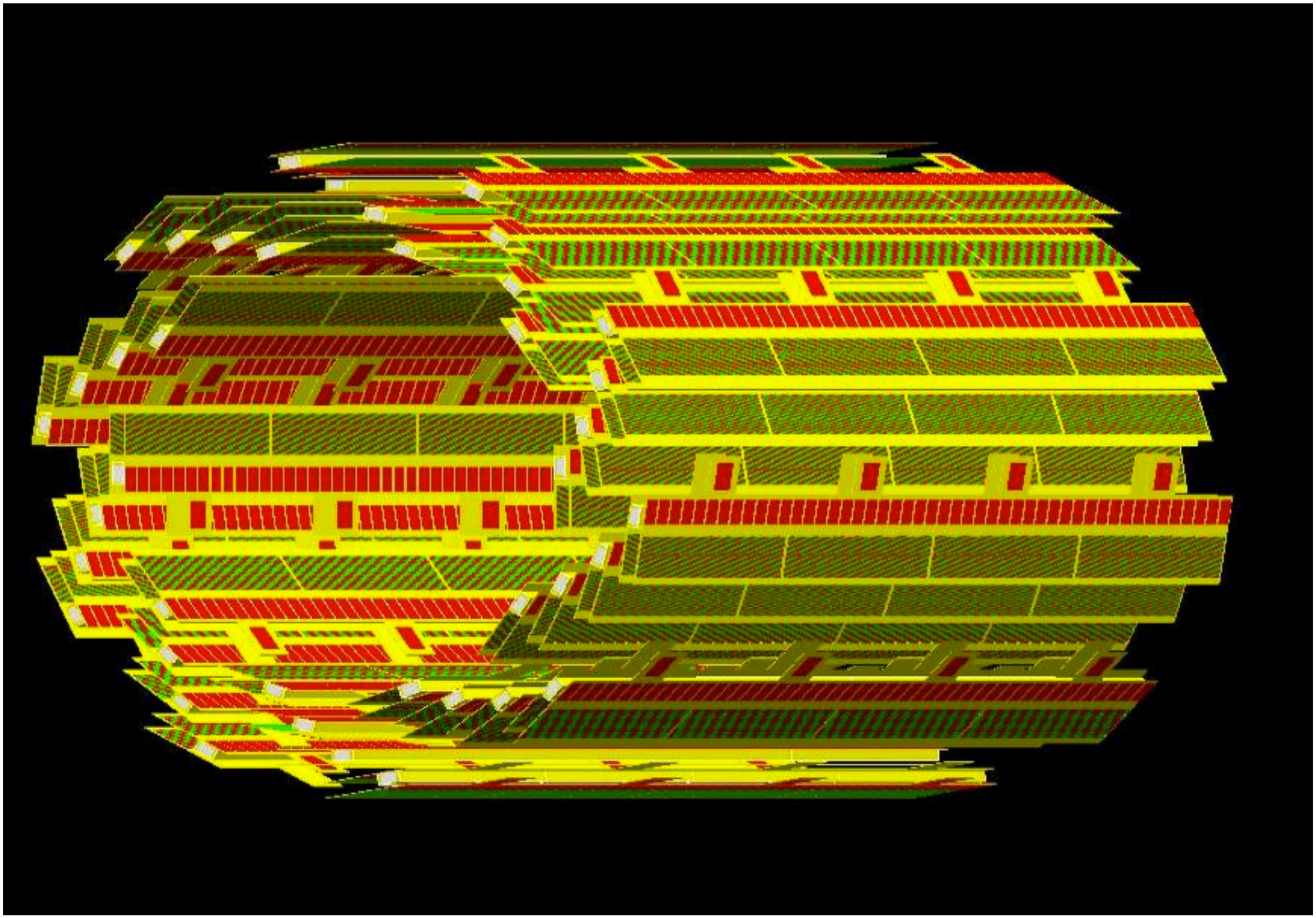
I presented some results from this in May, where I found a mass resolution of about 110 MeV for the ladder equivalent of the revised MIE configuration (roughly 10% worse than for the cylinder cell model).

Note that - unlike the cylinder cell model - the ladder model requires that there be some **overlap** of the sensors in phi to avoid ineficiency for curving tracks. I was assuming 15% overlap in phi.

This necessarily makes the ladder geometry thicker on average than the cylinder cell geometry.

SVX4 version: Layers 0 and 1 (8.5 cm inner radius, 256 strips in Φ)

16 mm strips - all strips read out



Code reorganization

The ladder model code was written in such a way that it would have been messy to change it to describe Yasuyuki's proposed FPHX configuration.

- The cooling and support structure is very different
- There is no longer an FPGA

Changes to:
coresoftware/simulation/g4simulation/g4detector/
PHG4SiliconTrackerDetector
PHG4SiliconTrackerSubsystem

Changes:
I have just finished a reorganization of the code to make it modular, so that parts of the ladder can easily be switched off (FPGA), or substituted with a different geometry (support and cooling).

At the same time, I made it possible to completely define the geometry of the detector from the calling macro (G4_Svtx_ladders.C), including switching between SVX4 and FPHX configurations. There are now no hardcoded dimensions at all.

I am now ready to write a new module describing the FPHX support structure - this is the only task remaining.

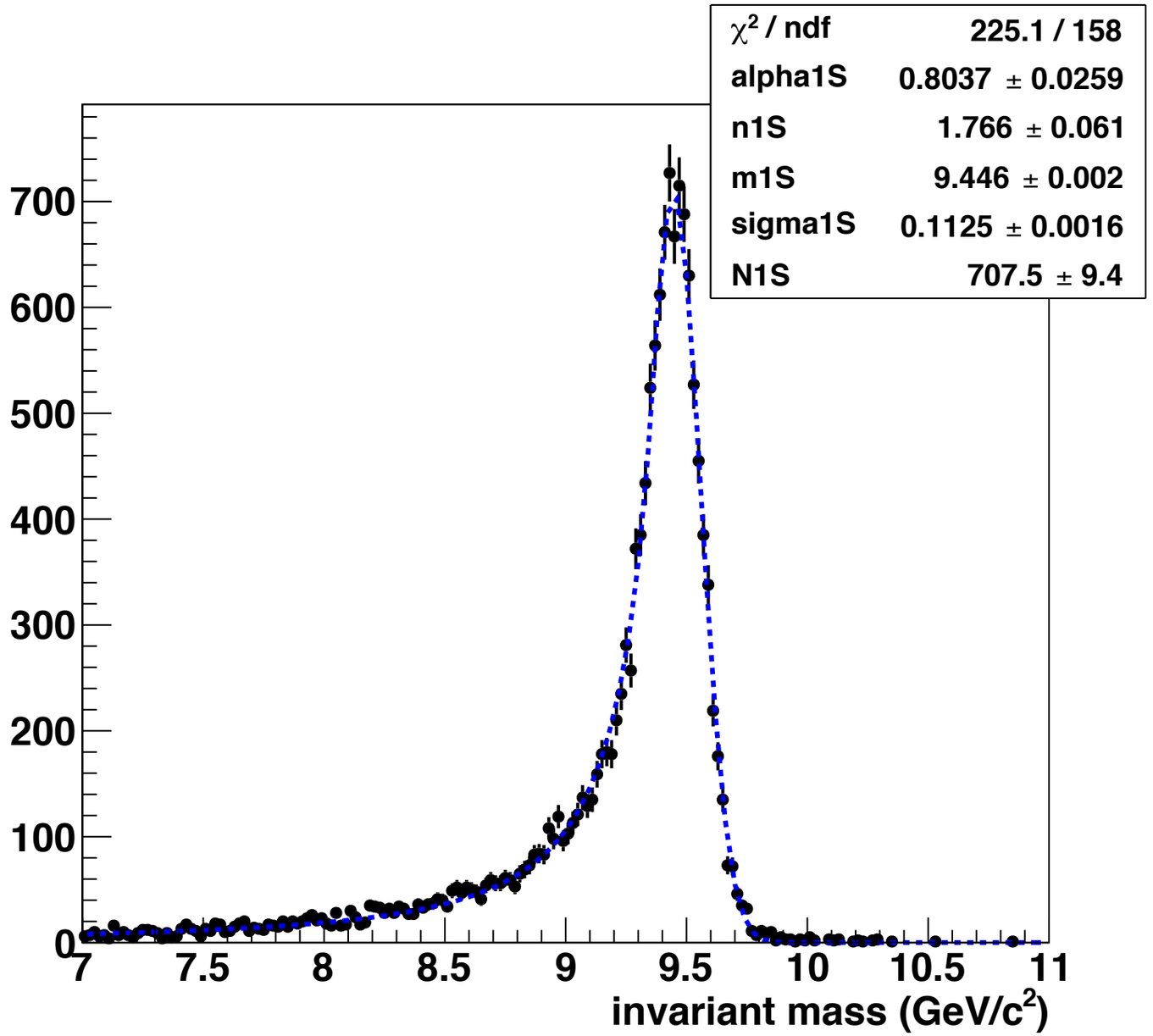
SVX4 chip ladder model

This is a calculation with the reorganized ladder construction code, for the SVX4 ladder version with the revised MIE radii.

This gives a resolution of 112 MeV.

Note however that the tracking code has not been re-optimized following some extensive rewrites, so this may not be the final word.

Mike is working on that.



What next?

Commit all changes to a development branch.

Merge with the main branch?

Implement the new cooling and support structure. Should take a couple of days.

Optimize the tracking for the new configuration.

Study and optimize pattern recognition
  -- Note that we cannot read out every strip, so some strips will be connected together. This is a pattern recognition issue.